Vitronics Soltec

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Wave soldering of SOICs

Introduction

SOICs are originally developed for reflow soldering. In the late 80's of the last century tests were done on 1.27 mm pitch SOICs, to find layout rules for wave soldering such components with a chipwave. The reason was a commercial one. The suppliers of such components supported and promoted any application in order to sell more of these components.

Therefore they provided layout rules for wave soldering; using extra pads at the drainage edge of the component in order to collect the solder that otherwise could give bridge formation on the last joints.

The tests that were done to provide these design rules were made on PCBs, on which only these components were mounted. So no other components such as SMD capacitors or resistors, or other joints were adjacent to these SOICs.
During these tests the optimal padsize for such components were found and these dimensions were published as the design rules for wave soldering.
Please note that these pad dimensions and the use of the extra drainage pads are different of the design rules for reflow soldering! If only one set of design rules are given, they are for reflow soldering only. Never use the reflow design rules for wave soldering applications. The outcome in solderbridging will often be disastrous.

Practical cases

The use of SOICs with a 1.27 mm pitch in wave soldering has always been tricky. The reason is that the capillary forces that make a solderjoint are relatively strong in-between joints with a fine pitch. This means that the solder tends to stay in-between the leads of adjacent joints. As long as the flow is not interrupted by adjacent components, the drainage conditions are often sufficient to prevent solderbridging, provided the correct drainage pad layout is used.
In case however that adjacent or neighboring components affect the solderflow on the SOIC, there is a big risk that solderbridging on the SOIC-leads will occur, in spite of the use of solder drainage pads.

The same story is valid for QFPs. Also these can be wave soldered, provided the correct layout for wave soldering is used. However as soon as solderjoints or components are close to these QFP solderjoints, the solder drainage conditions may change, resulting in solderbridging.
These effects have never been tested by the component suppliers, they are however very relevant for the practical cases were users are faced with the fact that however they used the correct design rules for wave soldering these SMDs, they still are faced with solder bridging.
Now we know were these frustrations come from. The point is however that the process can never compensate for a poor design.

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For SOIC components with a finer pitch than 1.27 mm, there is no practical experience with wave soldering. Knowing the previous problems regarding the drainage conditions we would never advise to use such components for wave soldering. So far we have seen no wave soldering layouts for 0.65 mm pitch SOICs, nor do we have practical experience with wave soldering such SOICs. From a process point of view we would not recommend these components for wave soldering.

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